inVinci Semiconductor Corporation

I3GA020N10

100V N-Channel Power MOSFET

Product Summary

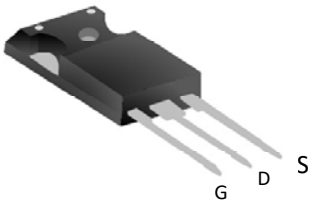
Parameter	Value	Unit
V_{DS} @ Tjmax	100	V
$R_{DS(on),max}$ @ V_{GS} = 10 V	2.0	mΩ
I_D @ V_{GS} = 10 V	305	A
P_{tot}	375	W

Features

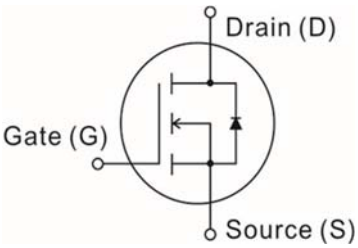
* Low on-resistance
* Low gate threshold voltage
* Excellent FOM

Application

* Synchronous rectification
* BMS battery protection
* DC/AC inverter
* DC/DC converter



TO-247



Maximum ratings T_A = 25℃ unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain - source voltage		V_{DS}	100	V
Continuous drain current	T_C @ 25℃	I_D	305	A
	T_C @ 100℃		215	
Pulsed drain current tp limited by Tj max (Note 1)	T_C @ 25℃	I_D pulsed	504	A
Single pulse avalanche energy (Note 2)		E_{AS}	1255	mJ
Gate-source voltage		V_{GS}	± 20	V
Power dissipation	T_C @ 25℃	P_{tot}	375	W
Storage temperature range		T_{STG}	- 55 to +175	℃
Operating junction temperature range	T_C @ 25℃	T_J	- 55 to +175	℃

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Electrical characteristics T_A = 25℃ unless otherwise specified						
Parameter	**Test Conditions**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Off characteristics						
Drain-source breakdown voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	100	---	---	V
Gate-source leakage	V_{GS} = ± 20V, V_{DS}=0V	I_{GSS}	---	---	± 100	nA
Zero gate voltage drain current	V_{DS}= 100V, V_{GS}= 0V, Tj=25℃ Tj=125℃	I_{DSS}	--- ---	0.1 ---	1 100	uA
On characteristics						
Drain-source on-state resistance	V_{GS} = 10V, I_D = 100A, Tj=25℃	$R_{DS(on)}$	---	1.8	2.0	mΩ
Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(th)}$	2.0	3.0	4.0	V
Gate resistance	F = 1MHz, open drain	R_G	---	1.2	---	Ω
Dynamic and switching characteristics-						
Gate-source charge	V_{DD} = 50V, I_D = 100A V_{GS} = 0 to 10V	Q_{gs}	---	53	---	nC
Gate-drain charge		Q_{gd}	---	31	---	
Gate charge total		Q_g	---	155	---	
Turn-on delay time	V_{DD} = 50V, I_D = 100A V_{GS} = 10V, $R_{G,ext}$ = 1.6Ω	Td(on)	---	44	---	ns
Rise time		Tr	---	36	---	
Turn-off delay time		Td(off)	---	81	---	
Fall time		Tf	---	22	---	
Input capacitance	V_{GS} = 0V, V_{DS} = 50V , F = 1MHz	C_{iss}	---	11100	---	pF
Output capacitance		C_{oss}	---	1730	---	
Reverse transfer capacitance		C_{rss}	---	45	---	

Parameter	**Test Conditions**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Drain-source diode characteristics and maximum ratings						
Inverse diode forward voltage	I_S = 100A, V_{GS} = 0V	V_{SD}	---	0.9	1.2	V
Reverse recovery time	V_R = 50V, I_F = 100A, di_F / dt = 100A / uS	t_{rr}	---	95	---	ns
Reverse recovery charge		Q_{rr}	---	295	---	nC

Notes:

1. **Repetitive rating : pulsed width limited by maximum junction temperature.**
2. **V_{DD}=50V, starting Tj=25℃.**

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Thermal characteristics			
Thermal resistance junction-to-case	R_{thJC}	0.4	℃ / W
Thermal resistance junction-to-ambient	R_{thJA}	62	

Package Marking and Ordering Information

Type / Ordering Code	Package	Packaging	Related Links
I3GA020N10	TO-247	Tube	see Package outline

Electrical characteristics diagrams

Fig 1: Power dissipation
$P_{tot} = f(T_C)$

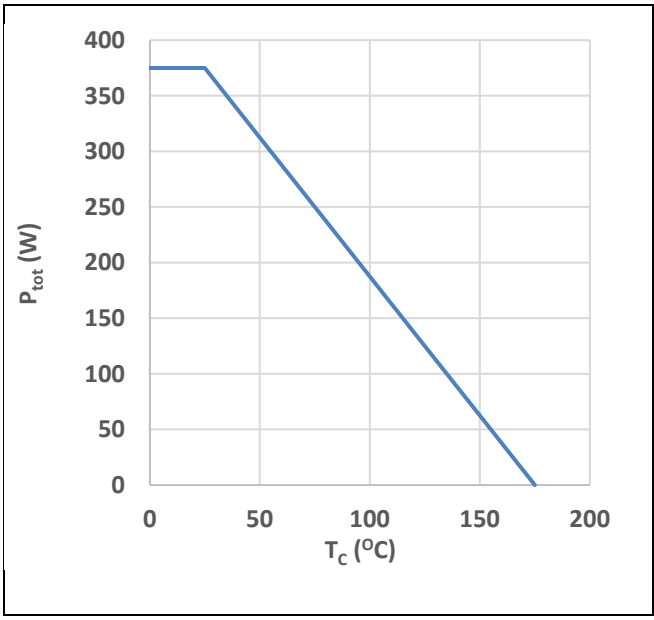


Fig 2: Safe operating area
$I_D = f(V_{DS})$; parameter : D = 0, T_C = 25℃

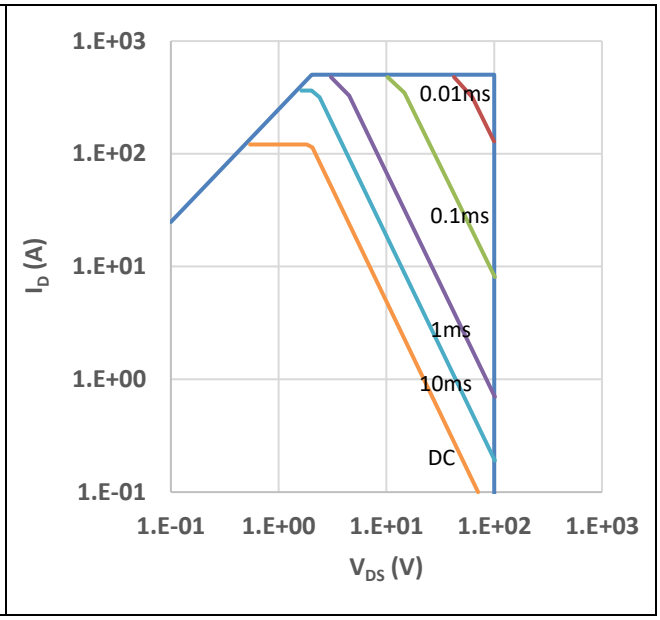


Fig 3: Transient thermal impedance
Z_{thJC} = f (tp); parameter : D = tp / T

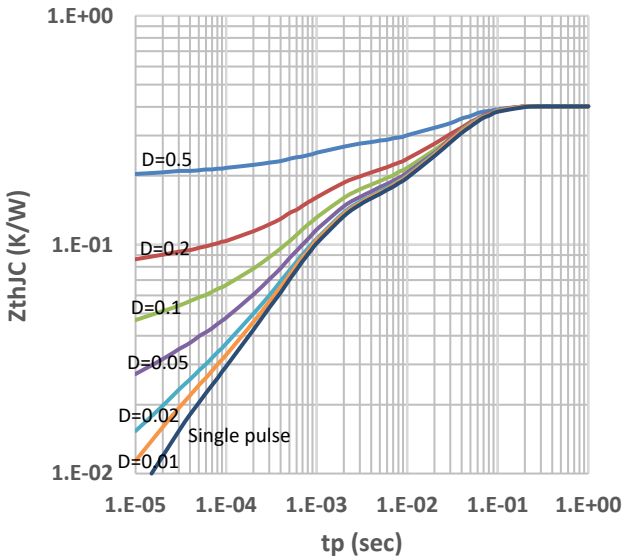


Fig 4: Typ. output characteristics
I_D = f (V_{DS}) ; Tj = 25℃; parameter: V_{GS}

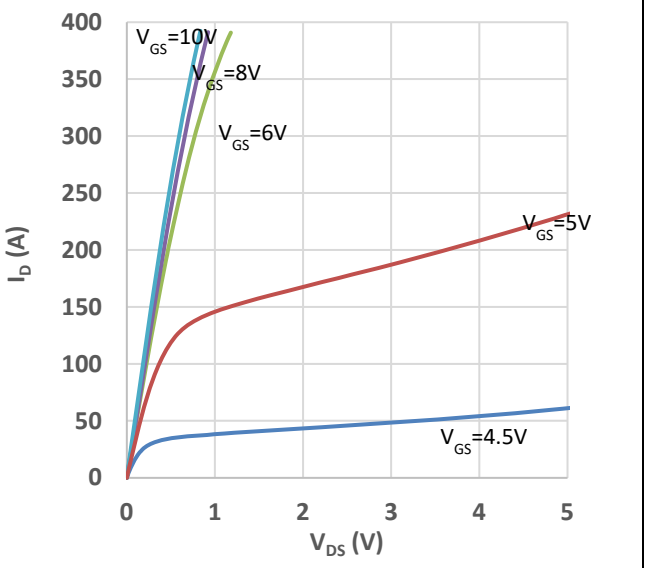


Fig 5: Drain current
I_D = f (T_C) ; V_{GS} >= 10V

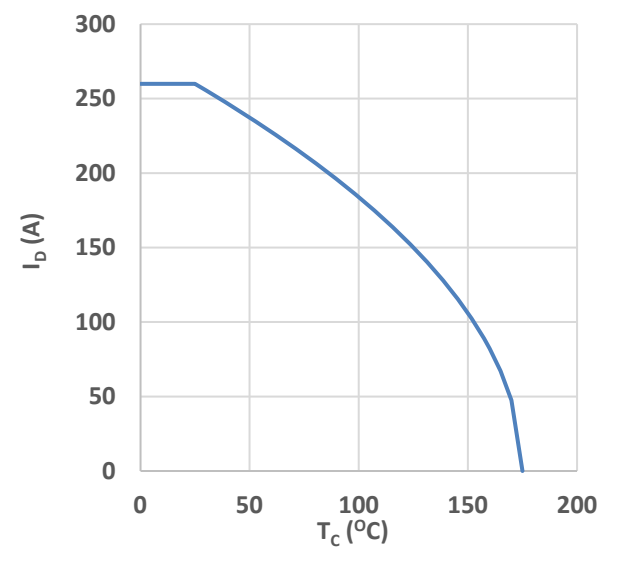


Fig 6: Typ. Drain source on-resistance
$R_{DS(on)}$ = f (I_D); parameter : tp = 50uS, Tj = 25℃, V_{GS}

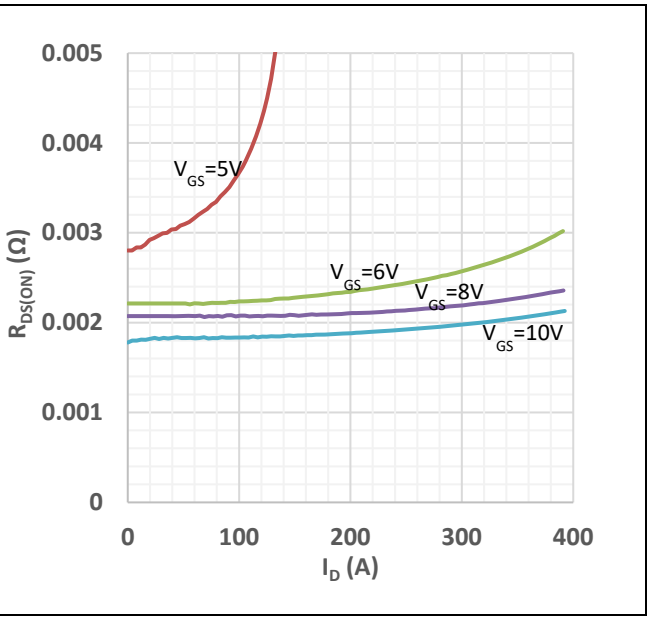


Fig 7: Drain-source on-state resistance
$R_{DS(on)}$= Tj ; parameter : I_D = 100A, V_{GS} = 10V

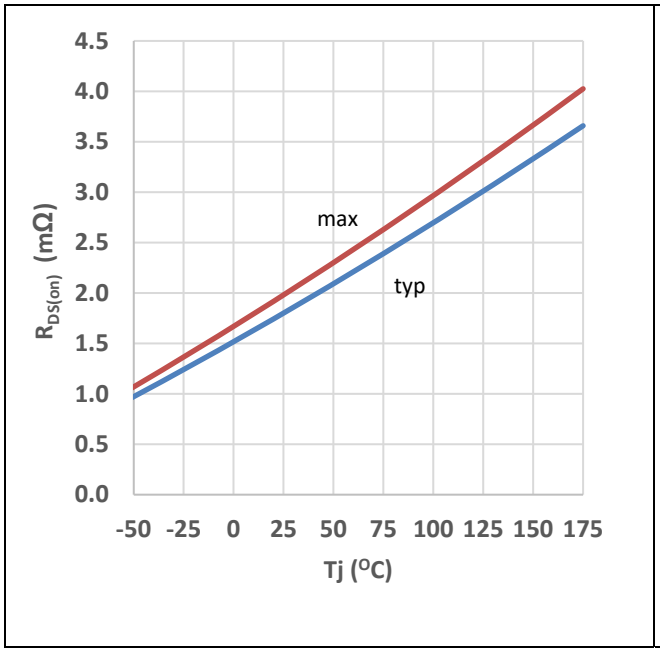


Fig 8: Typ. transfer characteristics
I_D = f (V_{GS}); V_{DS} ≧2 X I_D X $R_{DS(on)\ max}$; Tj = 25℃;
parameter : tp = 50 uS

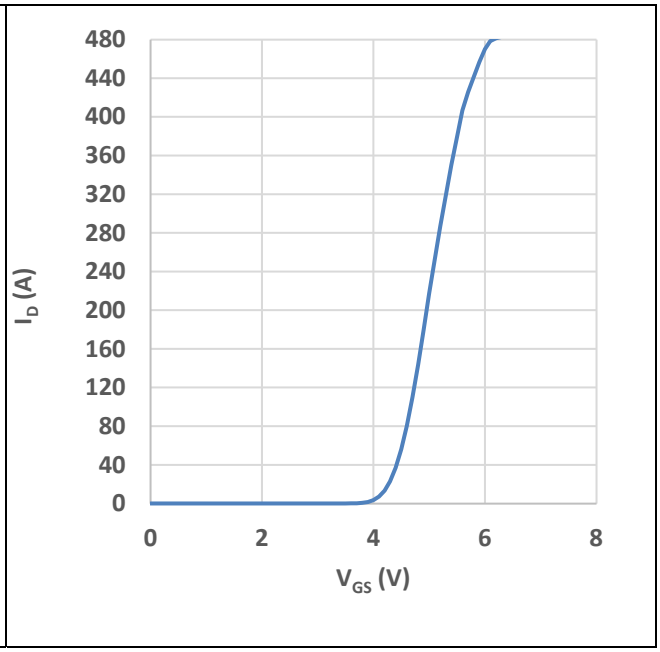


Fig 9: Typ. gate charge
V_{GS} = f(Q_{GATE}); I_D = 100A pulsed

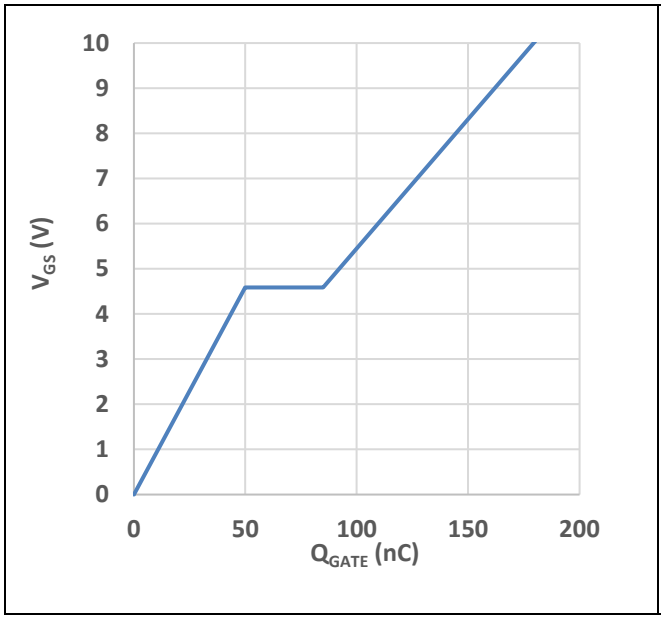


Fig 10: Forward characteristics of body diode
I_F = f(V_{SD}); parameter : Tj, tp = 20uS

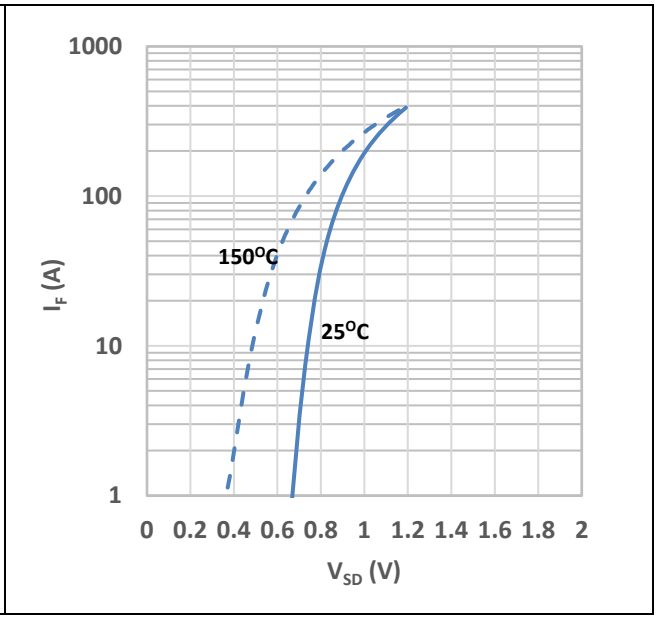


Fig 11: Drain-source breakdown voltage
$V_{(BR)DSS}$ = f(Tj)

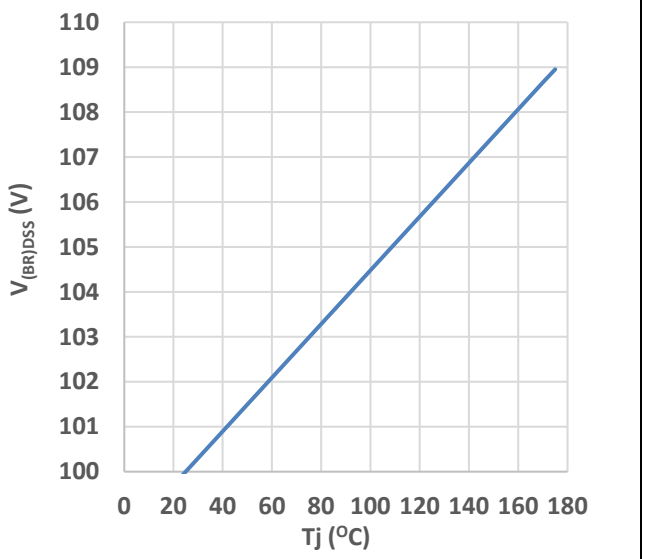


Fig 12: Typ. capacitances
C = f (V_{DS}); parameter : V_{GS} = 0V, f = 1MHz

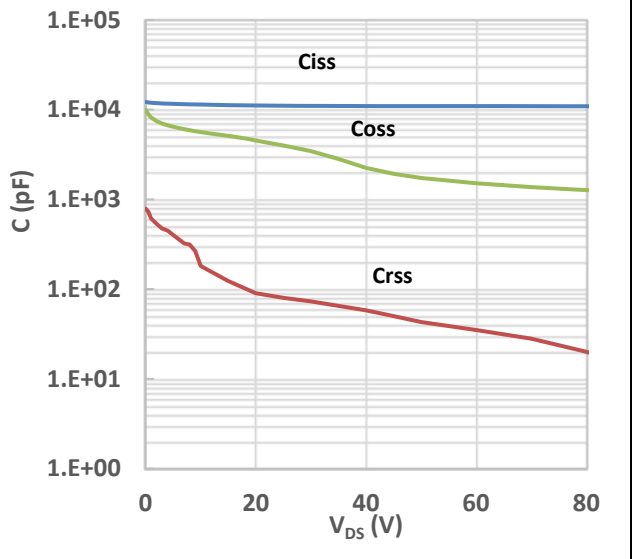
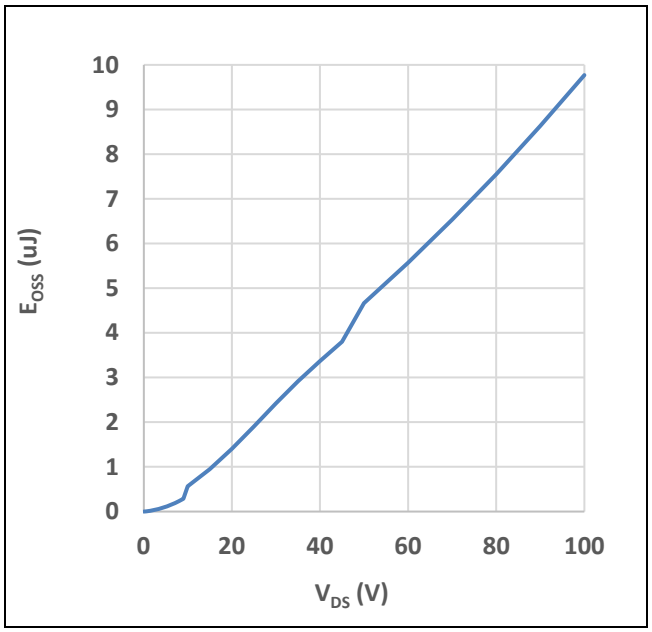
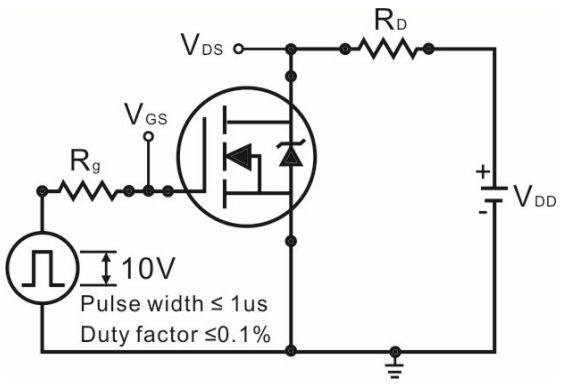
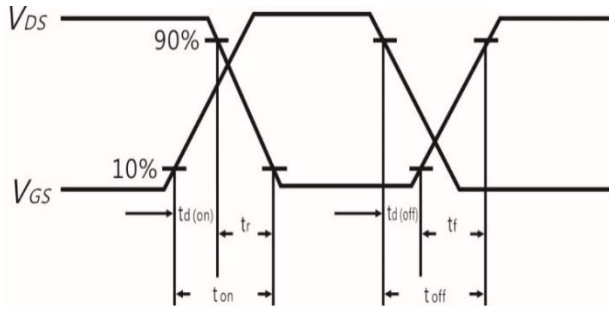
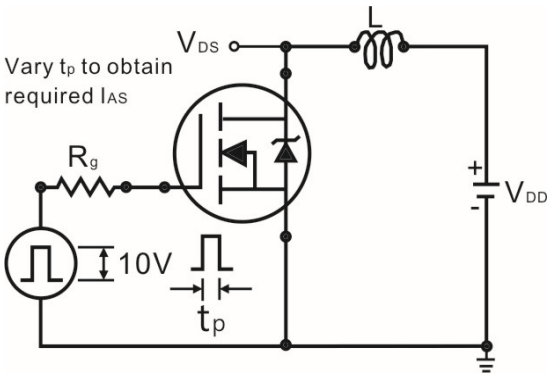
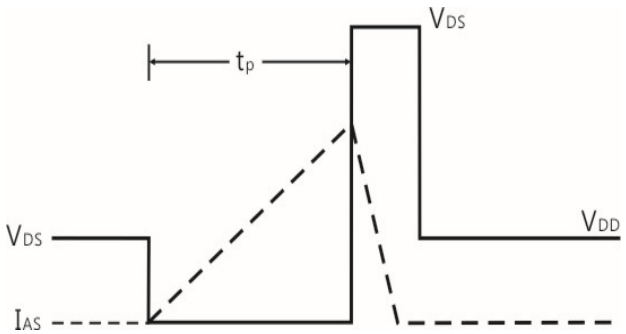


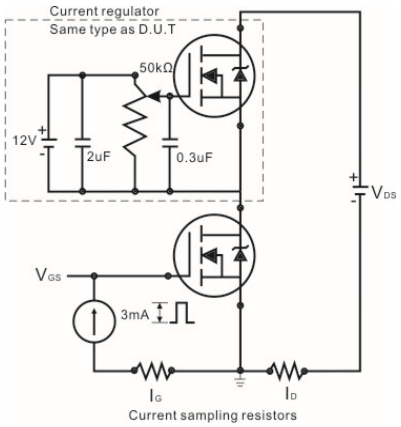
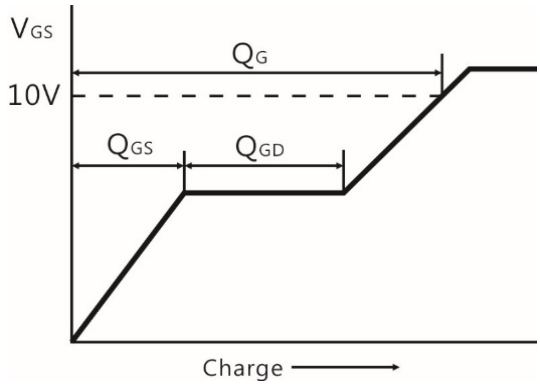
Fig 13: Typ. Coss stored energy
E_{oss} = f (V_{DS})



Test Circuit

Unclamped test circuit	Unclamped test waveform
	

Gate charge test circuit	Basic gate charge waveform
	

Diode recovery test circuit	Diode recovery test waveform
	

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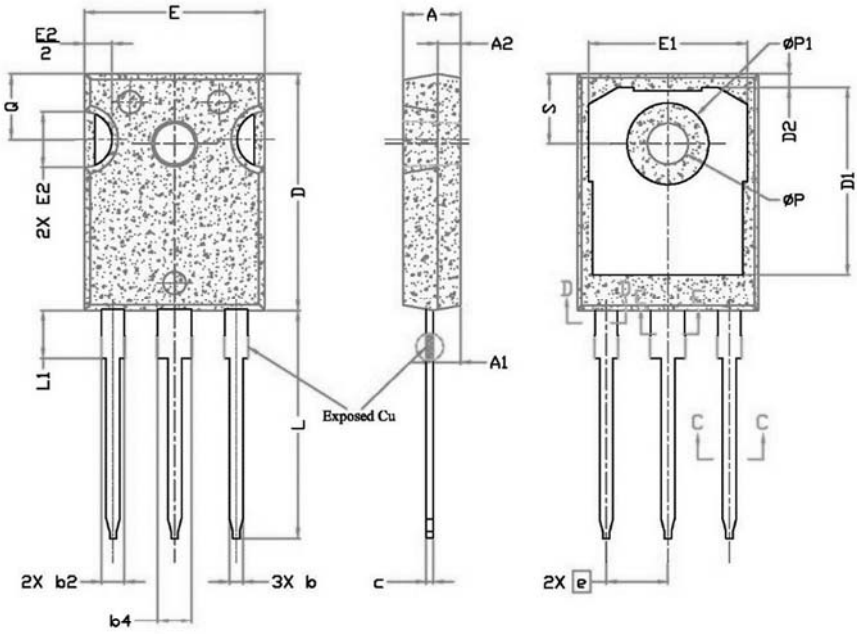
Package outline



Note:
1. Package Reference: JEDEC TO247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.
7. ØP To Have A Maximum Draft Angle Of 1.5° To The Top Of The Part With A Maximum Hole Diameter Of 3.91mm.
8. Dimension "b2" And "b4" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.10mm Total In Excess Of "b2" And "b4" Dimension At Maximum Material Condition.

SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e		5.44BSC		
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
ØP	3.56	3.61	3.65	7
ØP1		7.19REF.		
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	