inVinci Semiconductor Corporation

I3JM60N65QS

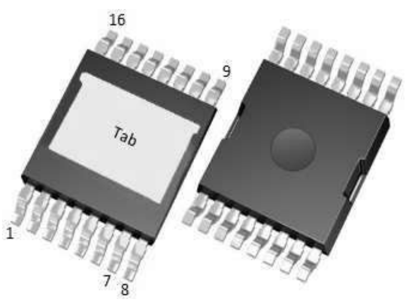
650V N-Channel Power MOSFET

Product Summary

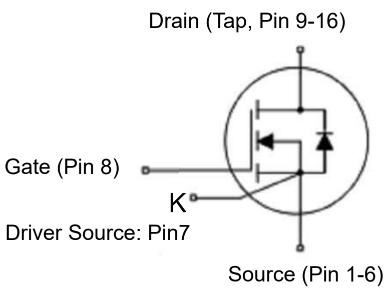
Parameter	Value	Unit
V_{DS} @ T_{jmax}	650	V
$R_{DS(on),max}$ @ V_{GS} = 10 V	48	mΩ
I_D @ V_{GS} = 10 V	60	A
P_{tot}	350	W

Features

* Multi-Epi process SJ-FET
* Low RDS(ON)
* Ultra Low Gate Charge
* E100% UIS and RG Tested
* Fast-Recovery body diode



TOLT



Application

* Power factor correction（PFC）
* Switched mode power supplies (SMPS)
* Uninterruptible Power Supply（UPS
* Half bridge or Asymmetric half bridge or Series

Maximum ratings T_A = 25℃ unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain - source voltage		V_{DS}	650	V
Continuous drain current	T_C @ 25℃	I_D	60	A
	T_C @ 100℃		35	
Pulsed drain current tp limited by T_j max (Note 1)	T_C @ 25℃	I_D pulsed	240	A
Single pulse avalanche energy (Note 2)		E_{AS}	120	mJ
Gate-source voltage		V_{GS}	± 30	V
Power dissipation	T_C @ 25℃	P_{tot}	350	W
Storage temperature range		T_{STG}	- 55 to +150	℃
Operating junction temperature range		T_j	150	℃

Electrical characteristics T_A = 25℃ unless otherwise specified						
Parameter	**Test Conditions**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Off characteristics						
Drain-source breakdown voltage	V_{GS} = 0V, I_D = 0.25mA	BV_{DSS}	650	---	---	V
Gate-source leakage	V_{GS} = ± 30V, V_{DS}=0V	I_{GSS}	---	---	± 100	nA
Zero gate voltage drain current	V_{DS}= 650V, V_{GS}= 0V, T_j=25℃	I_{DSS}	---	---	5	uA
On characteristics						
Drain-source on-state resistance	V_{GS} = 10V, I_D = 30A, T_j=25℃	$R_{DS(on)}$	---	43	48	mΩ
Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(th)}$	3	4	5	V
Gate resistance	f = 1MHz, open drain	R_G	---	3.2	---	Ω
Dynamic and switching characteristics-						
Gate-source charge	V_{DD} = 400V, I_D = 30A V_{GS} = 0 to 10V	Q_{gs}	---	35	---	nC
Gate-drain charge		Q_{gd}	---	45	---	
Gate charge total		Q_g	---	110	---	
Turn-on delay time	V_{DD} = 400V, I_D = 30A V_{GS} = 10V, R_G=1.8Ω	$t_{d(on)}$	---	15	---	ns
Rise time		t_r	---	35	---	
Turn-off delay time		$t_{d(off)}$	---	87	---	
Fall time		t_f	---	6	---	
Input capacitance	V_{GS} = 0V, V_{DS} = 35V , f = 1MHz	C_{iss}	---	5300	---	pF
Output capacitance		C_{oss}	---	230	---	
Reverse capacitance		C_{rss}	---	17	---	

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Drain-source diode characteristics and maximum ratings						
Inverse diode forward voltage	I_S = 30A, V_{GS} = 0V	V_{SD}	---	0.95	1.5	V
Reverse recovery time	V_R = 400V, I_F = 30A, di_F / dt = 100A / uS	t_{rr}	---	180	---	ns
Reverse recovery charge		Q_{rr}	---	1.3	---	nC

Notes:

1. **Repetitive rating : pulsed width limited by maximum junction temperature.**
2. **V_{DD}=50V, starting T_j=25℃.**

Thermal characteristics			
Thermal resistance junction-to-case	R_{thJC}	0.36	℃ / W
Thermal resistance junction-to-ambient	R_{thJA}	40	

Package Marking and Ordering Information

Type / Ordering Code	Package	Packaging	Related Links
I3JM60N65QS	TOLT	Tape	See Package Outline

Electrical characteristics diagrams

Fig 1: Power dissipation
$P_{tot} = f(T_C)$

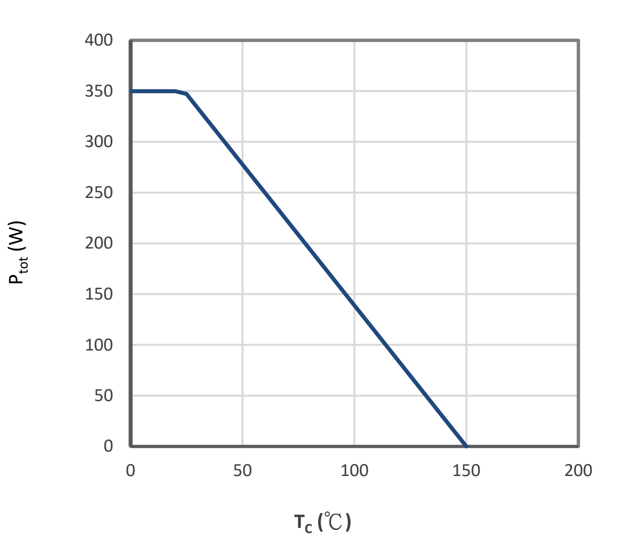


Fig 2: Safe operating area
$I_D = f(V_{DS})$; $V_{GS} > 10V$, $D = 0$, $T_C = 25℃$; parameter : tp

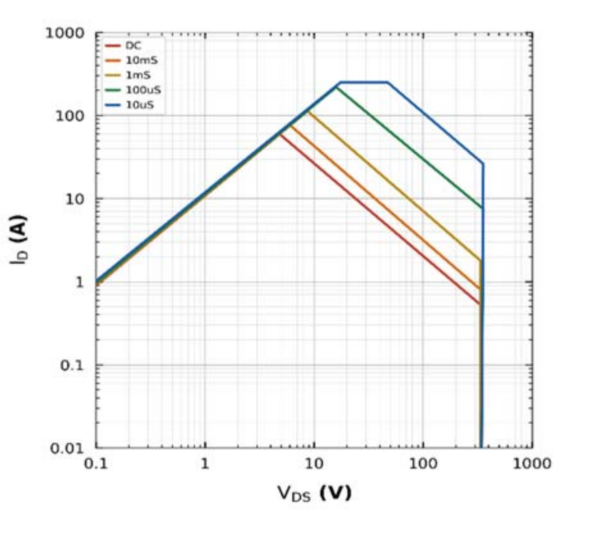


Fig 3: Typ. transfer characteristics

$I_D = f(V_{GS})$ C

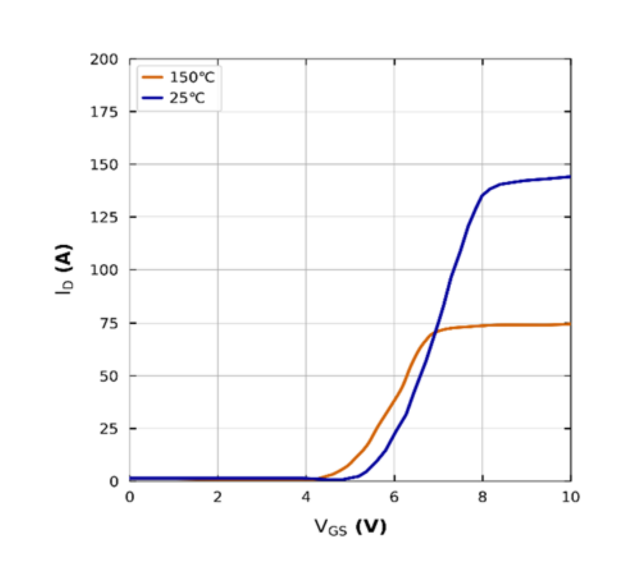


Fig 4: Typ. output characteristics

$I_D = f(V_{DS})$; T_j = 25℃ ; parameter : V_{GS}

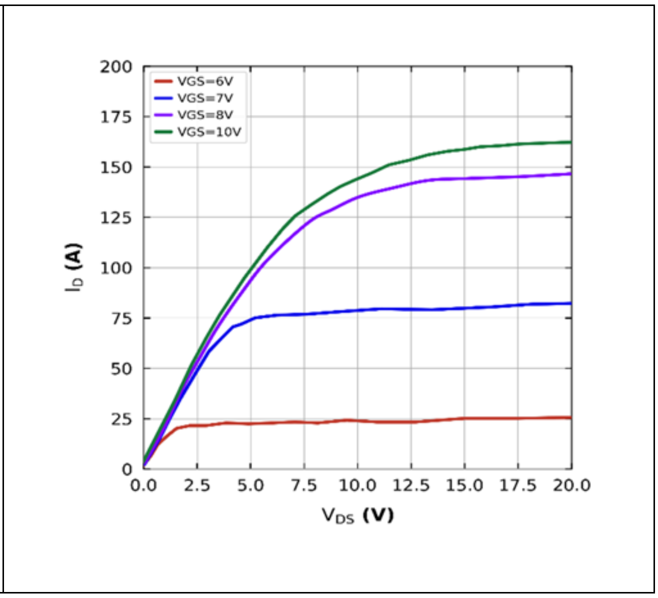


Fig 5: Forward characteristics of body diode

$I_F = f(V_{SD})$; parameter : T_j

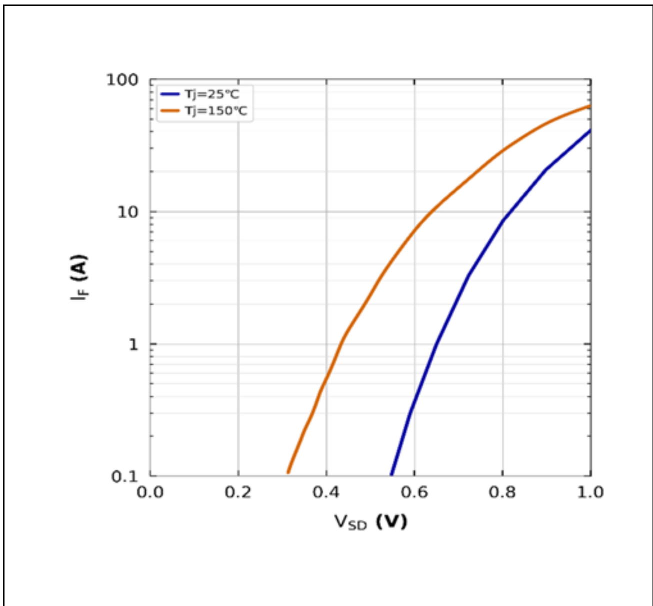


Fig 6: Typ. Drain source on-resistance

$R_{DS(on)} = f(I_D)$; T_j = 25℃ ; parameter : V_{GS}

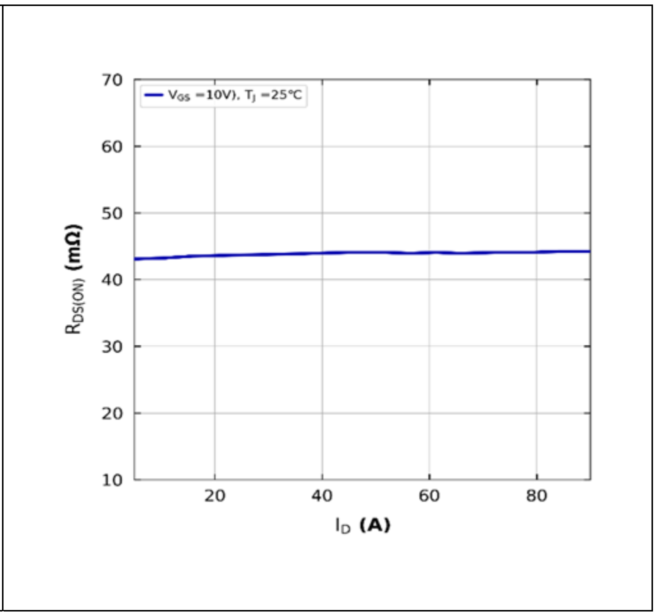


Fig 7: Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$; I_D = 30A, V_{GS} = 10V

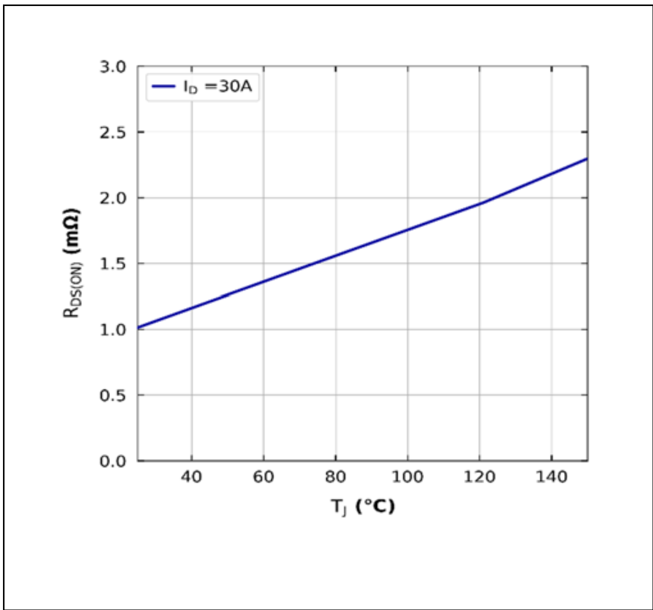


Fig 8: Typ. capacitances
$C = f(V_{DS})$; parameter : V_{GS} = 0V, f = 1MHz

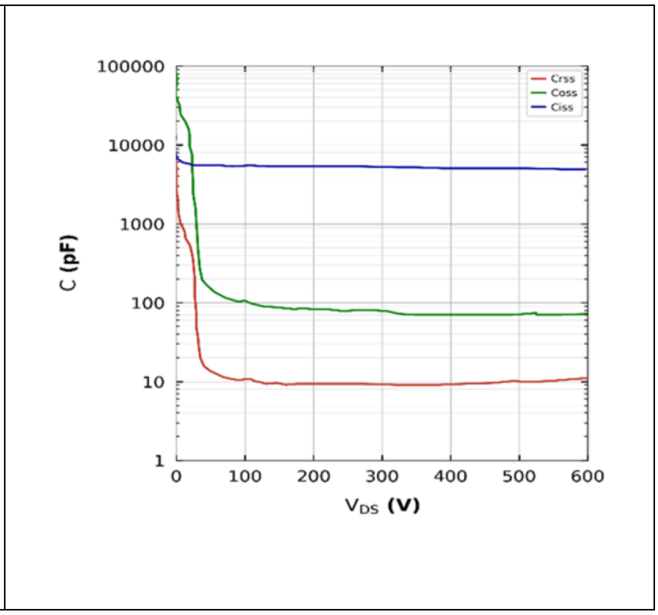
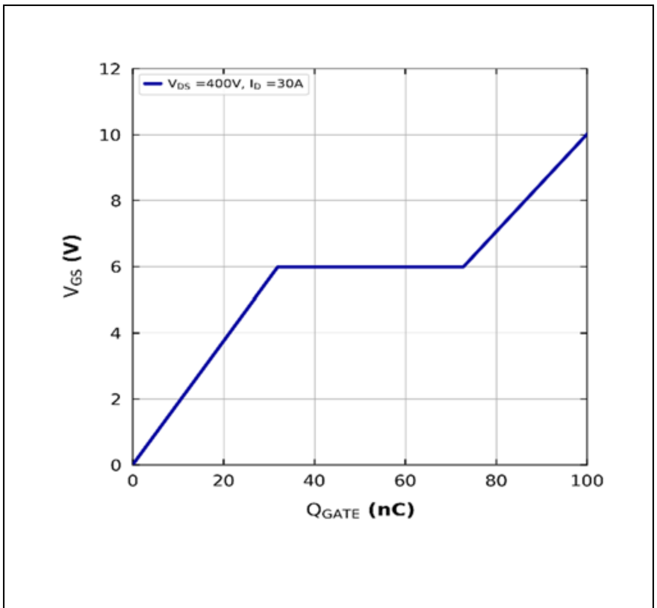
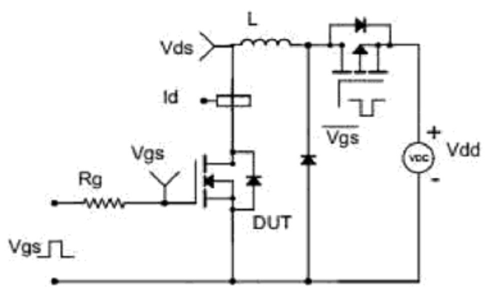


Fig 9: Typ. gate charge
$V_{GS} = f(Q_{GATE})$; I_D =30A pulsed

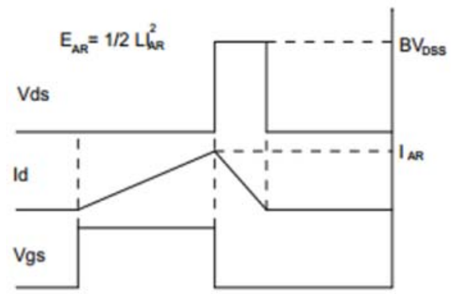


Test Circuit

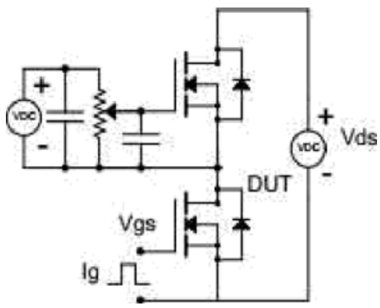
Unclamped test circuit



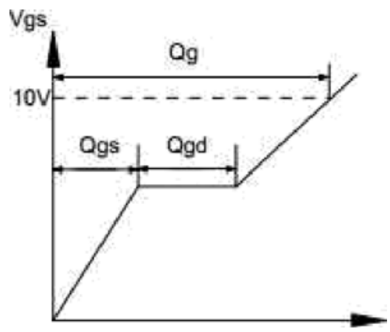
Unclamped test waveform



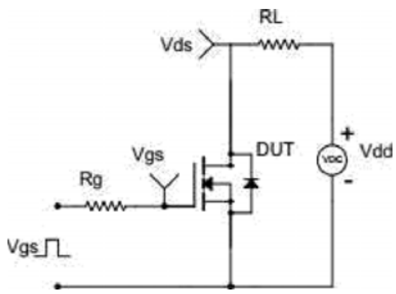
Gate charge test circuit



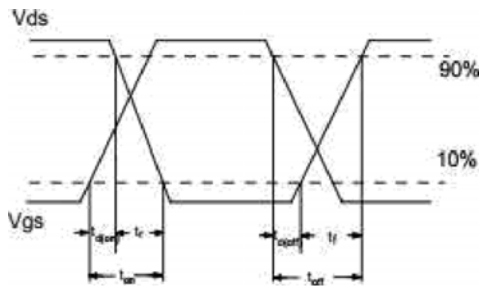
Basic gate charge waveform



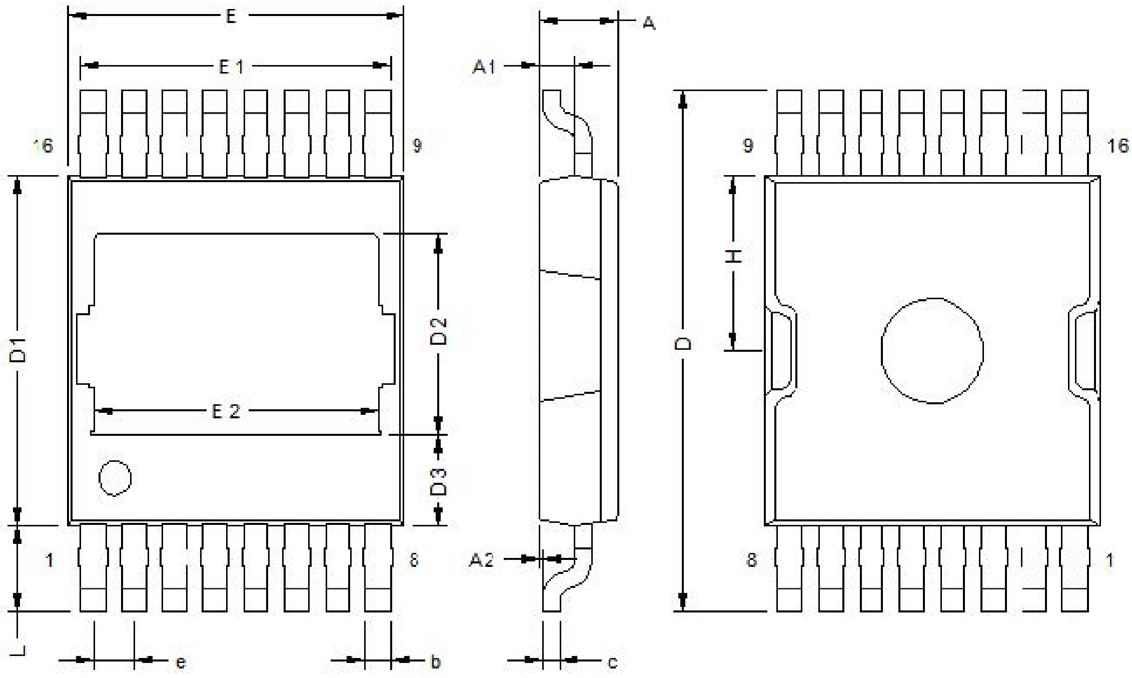
Switching test circuit (resistor load)



Switching test waveform



Package Outline



unit: mm

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	2.25	2.30	2.35	D3	2.5		3.0
A1	1		1.08	e	1.18	1.20	1.22
A2	0.01		0.16	E	9.7		10.1
b	0.68	0.70	0.74	E1		9.1	
c	0.45	0.50	0.55	E2		8.2	
D	14.80		15.20	H	4.84		5.25
D1	10.00		10.30	L	2.40		2.50
D2		5.7					