invinci Semiconductor Corporation

I3JA30N65Q

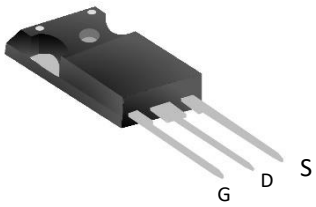
650V N-Channel Power MOSFET

Product Summary

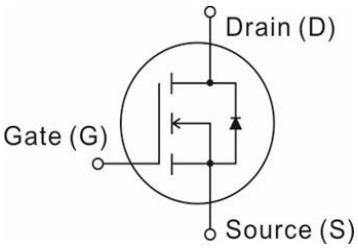
Parameter	Value	Unit
V_{DS} @ T_{jmax}	650	V
$R_{DS(on),max}$ @ V_{GS} = 10 V	120	mΩ
I_D @ V_{GS} = 10 V	30	A
P_{tot}	284	W

Features

* Low on-resistance
* Low switching losses
* Excellent FOM
* excellent stability and uniformity



TO-247



Application

* PC power
* Server power
* EV charger
* LED lighting
* UPS

Maximum ratings T_A = 25℃ unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain - source voltage		V_{DS}	650	V
Continuous drain current	T_C @ 25℃	I_D	30	A
	T_C @ 100℃		19	
Pulsed drain current tp limited by T_j max (Note 1)	T_C @ 25℃	I_D pulsed	90	A
Single pulse avalanche energy (Note 2)		E_{AS}	850	mJ
Gate-source voltage		V_{GS}	± 30	V
Power dissipation	T_C @ 25℃	P_{tot}	284	W
Storage temperature range		T_{STG}	- 55 to +150	℃
Operating junction temperature range		T_j	- 55 to +150	℃

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Electrical characteristics T_A = 25℃ unless otherwise specified						
Parameter	**Test Conditions**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Off characteristics						
Drain-source breakdown voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	650	---	---	V
Gate-source leakage	V_{GS} = ± 30V, V_{DS}=0V	I_{GSS}	---	---	± 100	nA
Zero gate voltage drain current	V_{DS}= 650V, V_{GS}= 0V, T_j=25℃	I_{DSS}	---	---	5	uA
On characteristics						
Drain-source on-state resistance	V_{GS} = 10V, I_D = 15A, T_j=25℃	$R_{DS(on)}$	---	105	120	mΩ
Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(th)}$	2.5	3.8	4.5	V
Gate resistance	f = 1MHz, open drain	R_G	---	12.5	---	Ω
Dynamic and switching characteristics-						
Gate-source charge	V_{DD} = 400V, I_D = 15A V_{GS} = 0 to 10V	Q_{gs}	---	19	---	nC
Gate-drain charge		Q_{gd}	---	20	---	
Gate charge total		Q_g	---	58	---	
Turn-on delay time	V_{DD} = 400V, I_D = 15A V_{GS} = 10V, R_G = 2Ω	$t_{d(on)}$	---	31	---	ns
Rise time		t_r	---	60	---	
Turn-off delay time		$t_{d(off)}$	---	102	---	
Fall time		t_f	---	58	---	
Input capacitance	V_{GS} = 0V, V_{DS} = 100V , f = 1MHz	Ciss	---	2500	---	pF
Output capacitance		Coss	---	100	---	

Parameter	**Test Conditions**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Drain-source diode characteristics and maximum ratings						
Inverse diode forward voltage	I_S = 15A, V_{GS} = 0V	V_{SD}	---	0.9	---	V
Reverse recovery time	V_R = 400V, I_F = 15A, di_F / dt = 100A / uS	t_{rr}	---	130	---	ns
Reverse recovery charge		Q_{rr}	---	0.85	---	uC

Notes:

1. **Repetitive rating : pulsed width limited by maximum junction temperature.**
2. **V_{DD}=50V, starting T_j=25℃.**

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Thermal characteristics			
Thermal resistance junction-to-case	R_{thJC}	0.44	℃ / W
Thermal resistance junction-to-ambient	R_{thJA}	80	

Package Marking and Ordering Information

Type / Ordering Code	Package	Packaging	Related Links
I3JA30N65Q	TO-247	Tube	see Package Outline

Electrical Characteristics Diagrams

Fig 1: Power dissipation
$P_{tot} = f(T_C)$

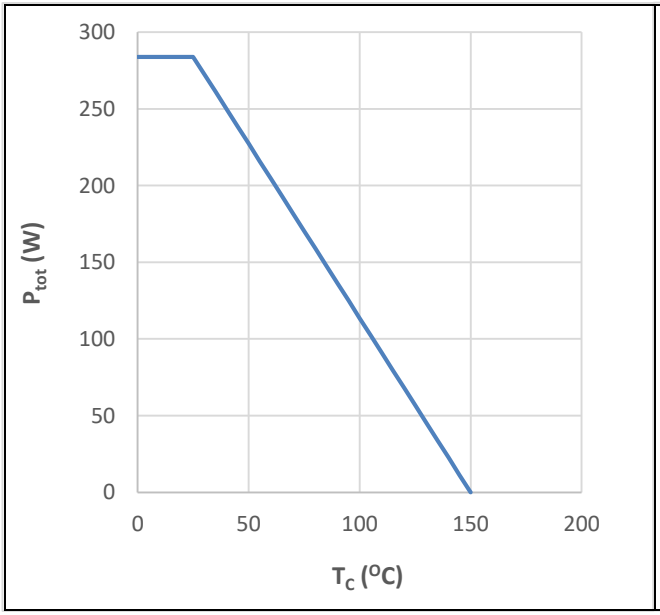


Fig 2: Safe operating area
$I_D = f(V_{DS})$; V_{GS} > 10V, D = 0, T_C = 25℃ ; parameter : tp

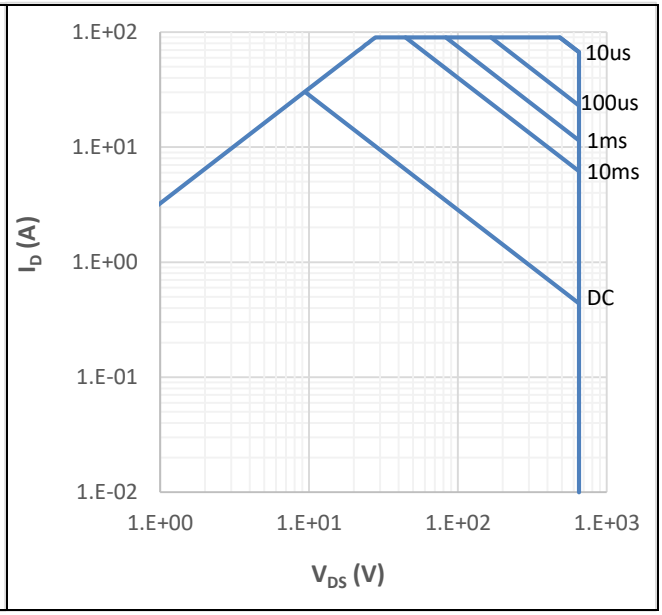


Fig 3: Typ. transfer characteristics
$I_D = f(V_{GS})$; $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, $T_j = 25^oC$

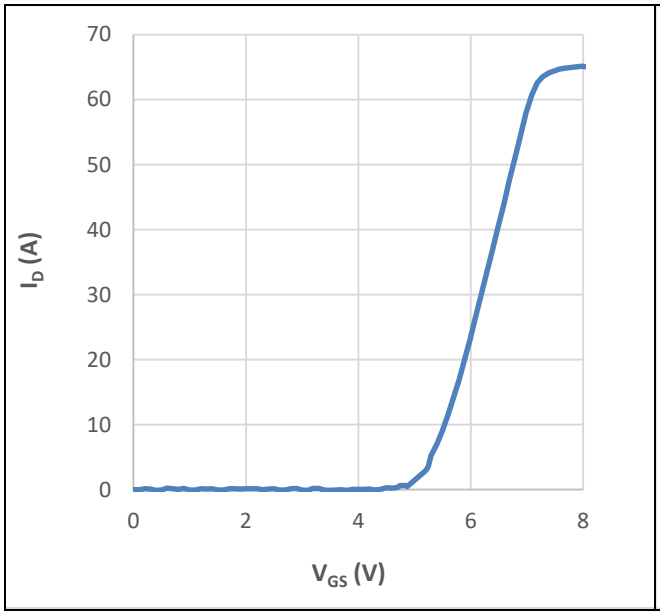


Fig 4: Typ. output characteristics
$I_D = f(V_{DS})$; $T_j = 25℃$; parameter : V_{GS}

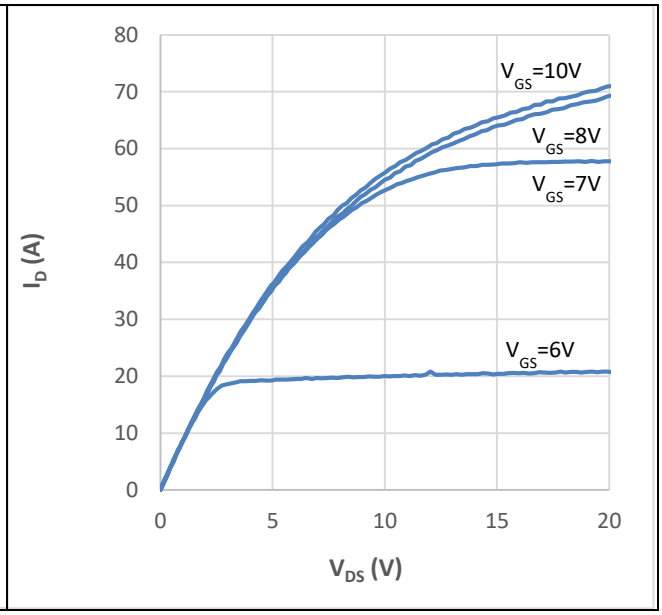


Fig 5: Forward characteristics of body diode
$I_F = f(V_{SD})$; parameter : T_j

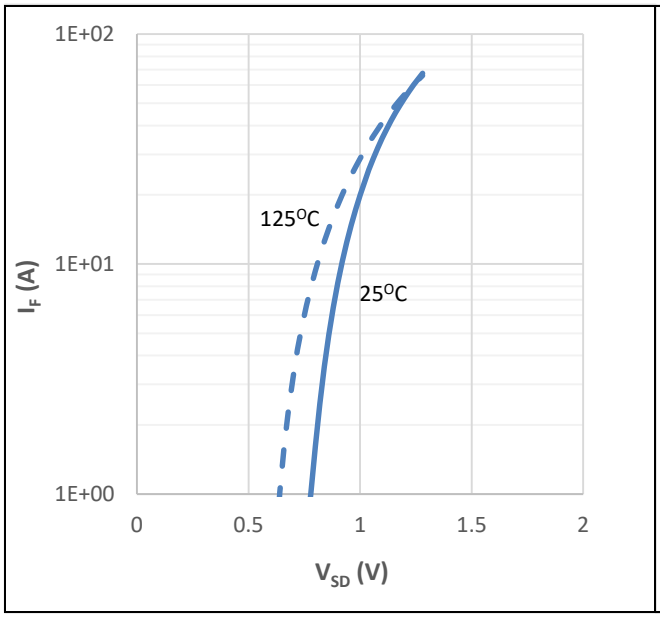


Fig 6: Typ. drain source on-resistance
$R_{DS(on)} = f(I_D)$; $T_j = 25℃$; parameter : V_{GS}

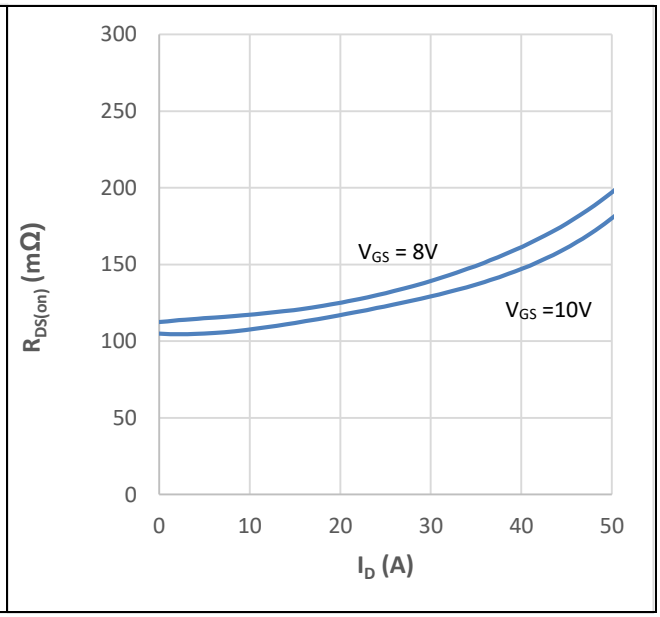


Fig 7: Drain-source on-state resistance
$R_{DS(on)}$ = f (T_j) ; I_D = 15A, V_{GS} = 10V

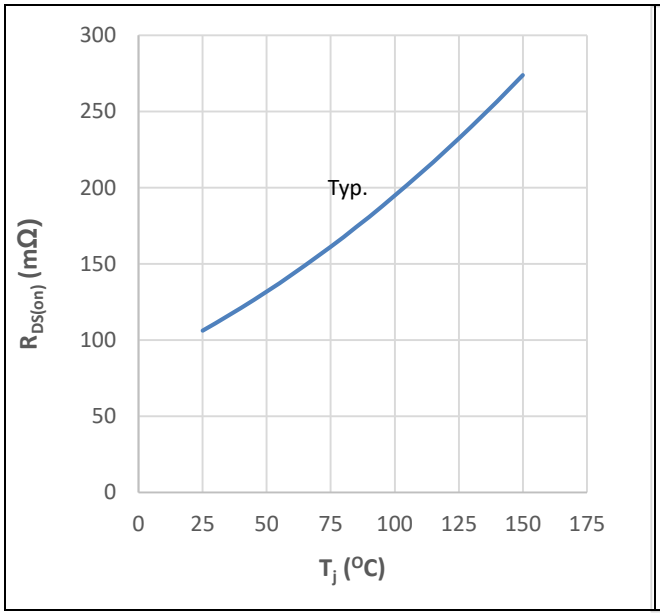


Fig 8: Typ. capacitances
C = f (V_{DS}); parameter : V_{GS} = 0V, f = 1MHz

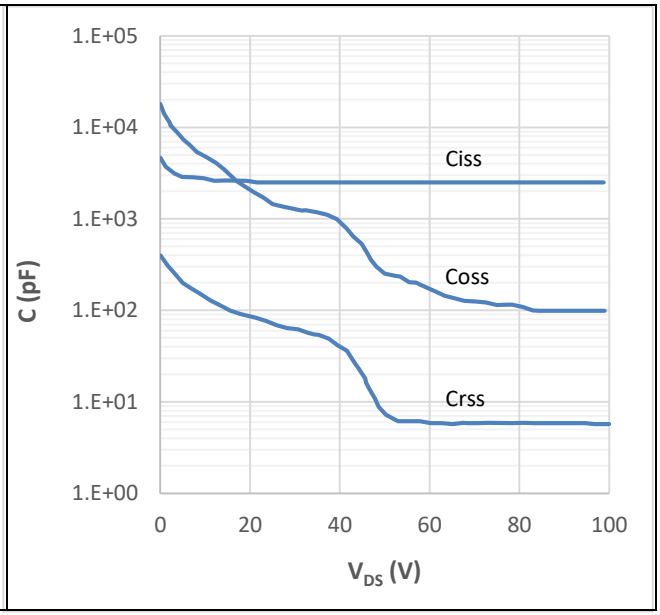
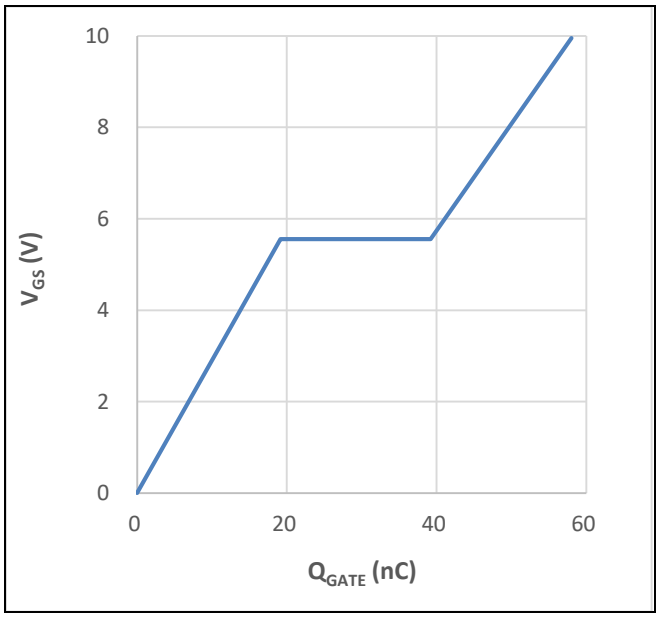
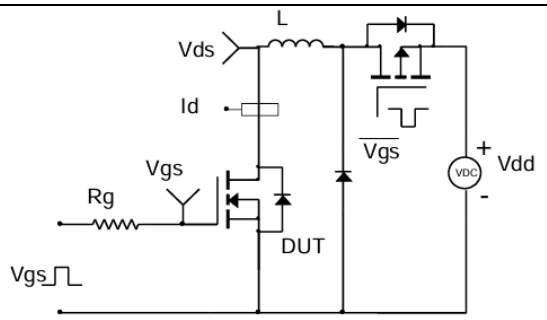
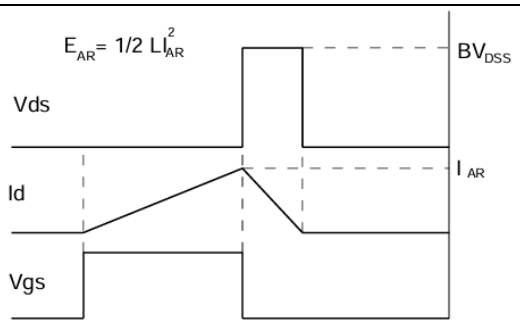
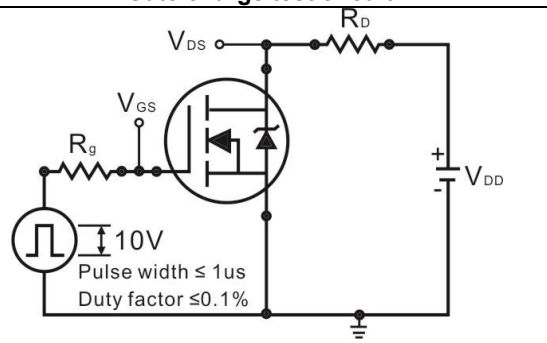
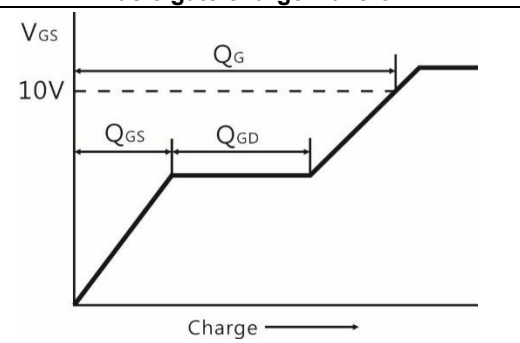


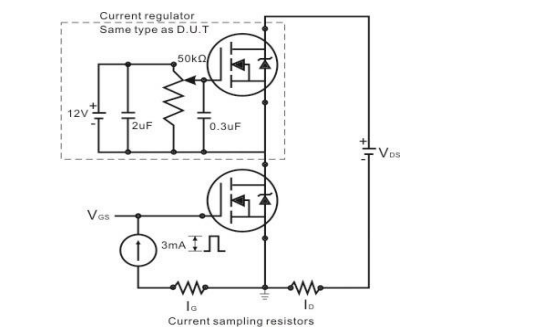
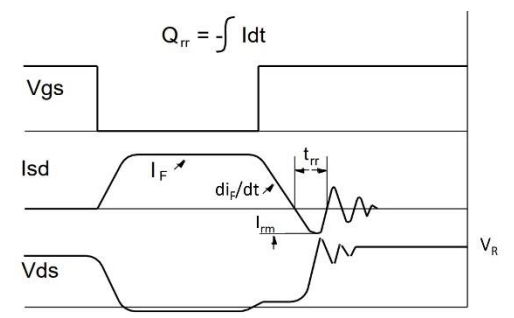
Fig 9: Typ. gate charge
V_{GS} = f (Q_{GATE}) ; I_D = 15A pulsed

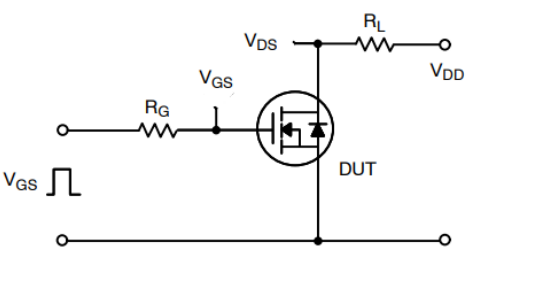
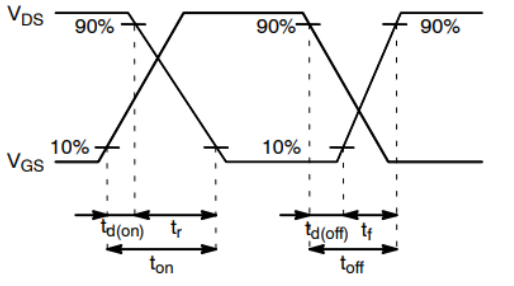


Test Circuit

Unclamped test circuit	Unclamped test waveform
	

Gate charge test circuit	Basic gate charge waveform
	

Diode recovery test circuit	Diode recovery test waveform
	

Switching test circuit (resistor load)	Switching test waveform
	

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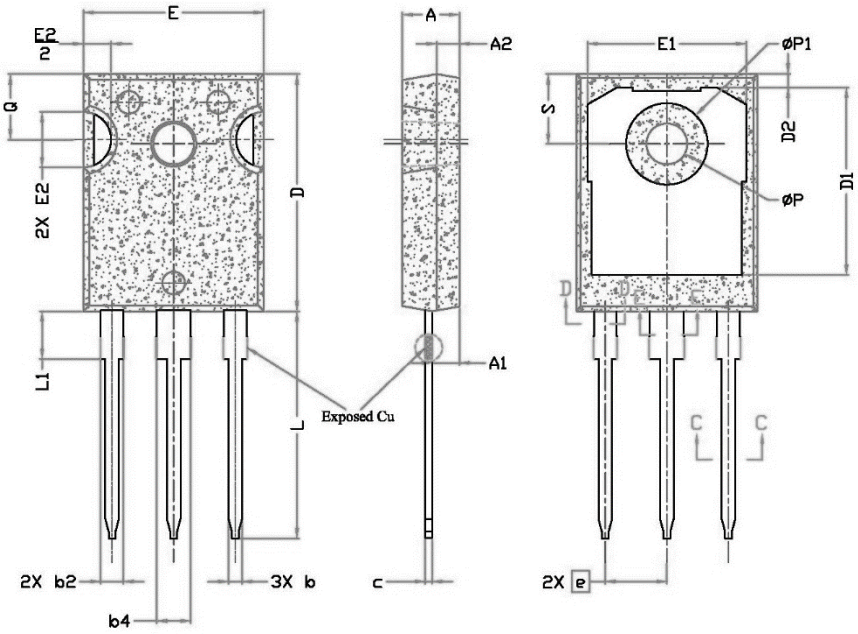
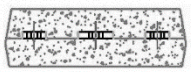
Package Outline





Note:
1. Package Reference: JEDEC TO247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.
7. ØP To Have A Maximum Draft Angle Of 1.5° To The Top Of The Part With A Maximum Hole Diameter Of 3.91mm.
8. Dimension "b2" And "b4" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.10mm Total In Excess Of "b2" And "b4" Dimension At Maximum Material Condition.

SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e		5.44BSC		
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
ØP	3.56	3.61	3.65	7
ØP1		7.19REF.		
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	